REMARKS

The Drawings were objected to due to an error in Figure 3. A replacement sheet for Figure 3 has been filed to correct the error. Applicants further file a replacement sheet for Figure 2.

Claims 1-9 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner has noted a number of issues. It is believed that the substantial amendments presented to the claims have addressed the Examiner's issues.

Claims 1-9 were rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. Applicants have amended the independent claims to recite a practical application (FIR filtering of input data) and the useful, concrete tangible result (the generation and output of filtered data). Withdrawal of the Section 101 rejection is requested.

Claims 1-9 were rejected under 35 U.S.C. 103(a) as being unpatentable over Giacalone. Claims 1-9 were rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata.

Turning first to claims 1 and 3, Applicants have moved the "without the need for delay lines" limitation from the preamble to the body of the claims. Applicants disagree with the Examiner's statement that this language is merely a recited purpose or intended use. Rather, in claim 1 this is a structural feature of the processing architecture and in claim 3 this is a limitation on the performance of the recited method.

Applicants have further emphasized in the claims that the specified unique partial product terms concern FIR partial products relating to the generation and output of filtered output values. Applicants submit that neither cited prior art reference teaches or suggests the claimed FIR filtering invention. Giacalone teaches a MAC environment with partial product calculation, and Iwata teaches a DSP environment with partial product calculation. However, neither cited reference teaches FIR filtering or the calculation of partial products comprising FIR partial products in an environment without delay lines or delay processing.

With respect to the specified unique partial product terms as claimed, the Examiner concedes that neither concedes that neither Giacalone nor Iwata teaches the limitation. The Examiner, however, points to paragraph 24 of Applicants' own disclosure which refers to Figure 2 of the application. This Figure 2 illustration and its associated description in paragraphs 24-25 of the specification are a part of and describe Applicant's invention. It is improper for the Examiner to rely on Applicant's disclosed invention as support in rejecting the claims. The

Examiner cannot use Applicant's disclosure as a roadmap for making modifications to the cited prior art in order to meet the recited claim limitations. The prima facie case for rejection under Section 103 cannot be made out through a combination of cited prior art (which does not teach a limitation) and the disclosure by Applicants of that limitation in the context of their own invention.

Claims 1 and 3 are accordingly asserted to be patentable over the cited prior art.

Turning next to claim 7, Applicants claim "the computation of certain specified unique partial product terms." As discussed above, the Examiner cannot rely on Applicants' own disclosure in meeting each claim limitation in support of a Section 103 rejection. On this basis alone, the rejection should be withdrawn.

Applicants further claim "wherein the partial product terms comprise a product of a certain one of a plurality of FIR filter coefficients and the given term of the input data." Applicants submit that neither cited prior art reference teaches or suggests the claimed FIR filtering invention. Giacalone teaches a MAC environment with partial product calculation, and Iwata teaches a DSP environment with partial product calculation. However, neither cited reference teaches FIR filtering or the calculation of partial products using FIR filter coefficients.

Claim 7 is accordingly asserted to be patentable over the cited prior art.

Dependent claims 8 and 9 are directed to the reuse of partial product terms, which were previously calculated in one iteration, in a later interation. The Examiner appears to suggest that this limitation is met by reference to paragraph 24 of Applicants' own specification. Again, for the reasons discussed above, this position is not proper. If the Examiner asserts that such reuse of partial products for FIR filtering is taught by either Giacolone or Iwata, Applicants request that the Examiner provide a specific prior art citation supporting this position.

Claims 8 and 9 are accordingly asserted to be patentable over the cited prior art.

Applicants have added new claims 10 and 11. Claim 10 is based on original claim 1, while claim 11 is based on original claim 3. Applicants submit these claims are patentable over the cited prior.

Claims 10 and 11 recite distributing computational load for the FIR filtering of input data across multiple processors by assigning to each processor the computation of specified unique partial product terms and the accumulation of computed partial product terms to generate filtered output sample values. The claimed partial product terms comprise a product of a certain

one of a plurality of filter coefficients and a certain term of the input data which is being FIR filtered. Applicants submit that neither cited prior art reference teaches or suggests the claimed invention.

Giacalone teaches a MAC environment with partial product calculation, and Iwata teaches a DSP environment with partial product calculation. However, neither cited reference teaches FIR filtering, the calculation of partial products comprising the product of filter coefficients and input data terms, or the distribution of computational load across processors in the manner claimed by Applicants. Applicants also claim a plural processor shared memory storing the input data to be FIR filtered and all filter coefficients. There is no teaching or suggestion in Giacolone or Iwata for the use of such a memory in the claimed FIR filtering operation. Applicants further point out that such a shared memory configuration facilitates linear scalability (as claimed), and there is no teaching that the Giacolone or Iwata processing architectures are linearly scalable.

In view of the foregoing, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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